IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:		
	Pankaj Kedia	
Serial No.:	09/753,326	Art Unit: 2116
Filed:	December 29, 2000	
		Examiner: Chen, Tse W.
For:	Low Power Subsystem For Portable Computers	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

APPEAL BRIEF
IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellant") hereby submit this Appeal Brief in support of its appeal from a final decision by the Examiner, mailed August 31, 2007 in the above-captioned case. This Appeal Brief is intended to support a third appeal initiated with a Notice of Appeal filed herewith. This third appeal is against the Examiner's non-final Office action of August 31, 2007, which was sent in lieu of a an Examiner's Answer to Appellant's second Appeal brief filed on February 6, 2007. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052-8119.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences that are related to, will directly affect, will be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF THE CLAIMS

Claims 29-56 are currently pending in this application. Claims 1-28 have been canceled. No claims have been allowed. All pending claims were rejected as obvious in the Office action mailed August 31, 2007 and are the subject of this appeal. No amendments have been submitted after that Office action.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on August 31, 2007, rejecting claims 29-56, Appellants file herewith a Notice of Appeal and this Brief.

A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Claims

Claim 29 is presented as a method with the following elements:

transitioning a central processing unit (CPU) (102 Page 4, line 9) of a computer system (100, Page 4, line 8) into a low power mode (See page 3, lines 3-6, lines 12-15,), the computer system having a memory (105 Page 4, line 18),

activating a low power subsystem (110 Page 5, line 11) when the CPU enters the low power mode, the low-power subsystem including a low power processor (111 Page 5, line 11), an external interface (115 Page 5, line 18) and a low power memory (113 Page 5, line 13);

independent of the CPU (See page 3, lines 7-10, , using the low power processor of the low power subsystem to access data contained within the computer system memory (See page 3, line 21-page 4, line 1, page 5, lines 17-22, page 6, lines 1-6, lines 15-16); and

providing the accessed data through the external interface of the low-power subsystem.

Claim 38 is presented as an apparatus with primarily the same features as Claim 29.

a computer system (100, Page 4, line 8) having a central processing unit (102 Page 4, line 9), a system memory (103 Page 4, lines 10-11), a mass storage device (105 Page 4, line 18), and a user interface, the computer system having a low-power mode (See page 3, lines 3-6, lines 12-15,); and

a low-power subsystem (110 Page 5, line 11) in operation when the computer system enters the low-power mode, the low power subsystem having a low power processor (111 Page 5, line 11), a low power subsystem memory (113 Page 5, line 13) and an external interface (115 Page 5, line 18) independent of the computer system, the low power processor providing access (See page 3, line 21-page 4, line 1, page 5, lines

17-22, page 6, lines 1-6, lines 15-16) to the computer system when the computer system is in the low power mode and the external interface providing data accessed from the computer system externally.

Claim 51 is directed only to the low power subsystem portion of Claim 29.

a miniature display screen (115, Page 5, lines 15-16);

a user input unit (this may be implemented through the Bluetooth interface 116 with an antenna 130 (See page 4, lines 2-4). A microphone may also be used (See page 7, lines 5-8));

a low-power subsystem memory (113 Page 5, line 13); and

a low-power processor (111 Page 5, line 11) coupled to the miniature display screen, to the user input unit, and to the memory, the low-power processor providing access (See page 3, line 21-page 4, line 1, page 5, lines 17-22, page 6, lines 1-6, lines 15-16) for the miniature display screen and the user input unit to a connected computer system (100, Page 4, line 8) when the connected computer system is in a low-power mode.

Background

The invention of Claim 1 may be easily understood in the context of the Background section of the present invention and in view of paragraph 5 which reads as follows.

"A low-power subsystem for a portable computer, which operates while the computer is in a low-powered mode in which the CPU performs in a less active state, is disclosed. Normally, when the notebook computer is in low power mode (also called powered down mode) during which the CPU is in a less active state and the notebook display screen may be in the closed position, the data stored within the computer typically cannot be accessed. One embodiment described herein allows access to the data while the computer is low power mode by use of a low-power subsystem (LPS) in the computer with access to the same memory storage as the CPU. The subsystem acts

independently of the CPU, which would not be able to perform the necessary functions during low power mode. The subsystem allows the notebook to perform several functions while in the low power mode, such as, for example, act like a travel assistant for the user, provide entertainment, and make electronic purchases."

VI. GROUNDS OF REJECTION

(A) Claims 29, 31 and 32 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, U.S. Patent 5,287,485 ("Umina"), in view of Barber, U.S. Patent No. 6,240,521 ("Barber").

(B) Claim 30 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, in view of Barber, and in further view of Kableshkov, U.S. Patent No. 6,108,663 ("Kableshkov").

(C) Claims 33-34, 36 and 37 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, in view of Barber, and in further view of Ditzik, U.S. Patent No. 5,983,073 ("Ditzik").

(D) Claim 35 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Ditzik, Umina, Barber, and in further view of Chen, U.S. Patent No. 5,590,197 ("Chen").

(E) Claims 38, 39, 40, 42, 44, 48-52 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over over Hollon, U.S. Patent No. 5,768,164 ("Hollon") in view of Umina.

(F) Claims 41, and 53 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Hollon and Umina in further view of Kableshkov.

Claims 54-56 are not rejected or addressed by the Examiner.

Grounds C, D and F are not argued below.

VII. ARGUMENT

A. Claim 29 is not obvious where neither reference teaches or suggests "using the low power processor of the low power subsystem to access data contained within the computer system memory."

Claims 29, 31 and 32 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, U.S. Patent 5,287,485 ("Umina"), in view of Barber, U.S. Patent No. 6,240,521 ("Barber"). Barber was relied on in the first Office action of November 20, 2003 and has remained the primary focus of the prosecution of the present application throughout. This rejection is identical to the rejection mailed by the Examiner on November 6, 2006 from which an appeal was also sought.

The Examiner would like to present this as a new rejection, however, it is not. The Examiner has cited Umina as showing (a) a computer system having a CPU 202 and a memory 204, and (b) a subsystem including a processor 206 and a memory 208. (The Examiner indicates that the subsystem is low power, but then writes that "Umina did not disclose low power operations...") Going back to November 20, 2003, this same Examiner on page 3 states that Barber shows the same thing. The combination of Barber with a reference that is relied on to show what was already stated to be in Dwyer is not a new rejection.

Umina has two SRAMs 204, 208 and two processors 202, 206. Both processors can access either SRAM, but only one at a time and only if the connections are reversed. (Col. 5, lines 41-62) Transfer logic 270 lies in between the two SRAMs described with respect to Figure 7, but not between the processors and the SRAMs. Umina, as suggested by the Examiner, has no low power operation. It is directed instead at high speed dual processor operation. The difference between Umina and Barber is that Umina shows two high power processors each with their own memory, while Barber, on the other hand has a low power processor that shares a single memory with a high speed processor.

Barber shows a conventional computer system with two processors 42, 44 coupled to a single I/O bus 46. In Barber, two processors share "a common instruction set and address space." "Since the two processors share a common address space, the contents of memory is available equally to both processors. It is only the machine state which must be passed back and forth between the active processor via the shared memory and the sleep mode transitions." (Col. 3, lines 43 et seq.)

In other words, the processors share everything. While this reduces the component price for the system, it increases the power consumption. In Barber, it provides for seamless transitions between the two processors.

In Claim 29, there are two processors but the low-power subsystem has its own memory. It also has its own external interface ("the low-power subsystem including a low power processor, an external interface and a low power memory"). Neither reference shows a whole subsystem. The components of the low power subsystem of the present invention may be optimized for low power operation, while the memory and external interface of the "computer system" may be optimized for speed. This costs more than reusing the same components but it provides a longer battery life. The low-power subsystem only has to access the "computer system" when data located there is desired.

Claim 29 further recites "using the low power processor of the low power subsystem to access data contained within the computer system memory." This draws a clear distinction between the computer system memory and the low-power subsystem memory. In Barber, there is only one memory, while in Umina, there is no low power subsystem.

Claim 29 further recites, "providing the accessed data through the external interface of the low-power subsystem." This operation is not possible with either reference as there is no separate external interface for the second processor.

In sum, neither reference shows a low power subsystem, only a second processor.

The Examiner could have argued that it would be obvious to apply the high power/low power system of Barber to the dual memory/dual processor system of Umina. Umina is directed to sharing data in the two memories between the two processors as quickly as possible. (See e.g. Col. 1, lines 50-65) Umina solves the problem using the transfer logic 270 that allows for direct transfer of data from one memory to another. Claim 29 recites, "using the low-power processor of the low-power subsystem to access data contained within the computer memory system." To the extent that this can be read on Umina. Umina considers this option and rejects it at Col. 1, lines 50-65 in favor of its transfer logic solution. To make such a modification of Umina then goes against the teachings of Umina and reduces its performance for the reasons that Umina provides.

The Examiner could have argued that it would be obvious to apply the dual memory/dual processor system of Umina to the high power/low power system of Barber. Barber, however, relies heavily on a saved machine state that is used to transition between the two processors (Abstract). Saving the current machine state in the shared address space allows for seamless transitions between the high and low power processors. Adding the second memory space would defeat the shared address space and defeat the entire purpose of Barber. The processors would no longer be able to make the seamless transitions.

If there is some way to add the memory and keep the shared address space, it is not described in either reference and it would require some significant design or engineering to accomplish. Umina does not discuss how to switch between processors but only contemplates using both processors at the same time and so provides no help in how to add a second memory without destroying the shared address space.

Neither singly, nor in combination, do the references teach or suggest the claimed invention. Accordingly, Appellants respectfully request that the Board reverse the Examiner's rejection of Claims 29, 31, and 32.

B. Claim 30 is not obvious where none of the references teach or suggest "a shared database with at least a partial copy of [the] data."

Claim 30 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Umina, in view of Barber, and in further view of Kableshkov, U.S. Patent No. 6,108,663 ("Kableshkov"). The application of Kableshkov to this claim is not new. This is also the same rejection that the Examiner presented in the prior November 6, 2007 Office action from which an appeal was also sought. Claim 30 refers to "accessing data comprises accessing data through a shared database of the low-power subsystem, the method further comprising storing at least a partial copy of data accessed from the computer system memory in the shared database."

Kableshkov was cited as showing a shared database. Presumably, the Examiner is referring to the host processor's 30 local cache memory 31. This memory 31 contains a copy of all or part of the database on the disk storage 34. The co-processor 44 (database engine) is able to access both the disk 34 and the cache 31 through the I/O bus 32. It would appear that this is allowed to increase the speed of the co-processor's operations.

However, Kableshkov does not show a shared database as recited in Claim 30. On the contrary, Kableshkov has no low-power mode and no suggestion that one should be provided. There is further no mode suggested in which one processor access data while the other processor sleeps.

This does not correspond to a shared database through which access to a computer system may be provided. It does not suggest a computer system memory, a low-power subsystem memory, and a shared database in combination.. Further, there is nothing in any of these three references to suggest modifications to accomplish such a thing. There is also nothing in any of the references to suggest applying such a database to allow a high speed processor to remain in a low power state.

Appellants accordingly request that the rejection of Claim 30 also be reversed.

C. Claims 38 and 51 are not obvious when neither reference suggests "a low power subsystem memory" nor providing access to a connected computer system when the connected computer system is in a low-power mode'"

The Examiner has rejected claims 38, 39, 40, 42, 44, 48-52 under 35 U.S.C. §103 (a) as being unpatentable over Hollon, Jr., U.S. Patent No. 5,768,164 ("Hollon") in view of Umina. This is the first rejection of the August 31, 2007 rejection that can be characterized as "new." However, Hollon was fully addressed in response to a March 1, 2005 rejection and also a June 20, 2005 rejection.

Hollon shows a small external user interface (screen and buttons) in Figure 2 that can be used when the notebook computer is folded. However, as shown in Figures 8 and 9, the "spontaneous use display" uses the same CPU, video controller and main memory as the main display and keyboard. ASIC 84 is used to map pixels of the main display to the "spontaneous use display." Accordingly there is no low power subsystem and no shared database coupled to both.

Hollon mentions power consumption as an issue in the Background section, however, Hollon does not address the problem. In order to operate the mini-display, and special function keys when the lid is closed, at least the main CPU 81, main video controller 83, I/O controller 91 and keyboard controller 92 must all be operating. In addition, the special mini-display ASIC 84, and the mini-display must be operating. The mini-display system will not operate if the CPU 81 is in a standby, sleep or hibernation mode because it is the only CPU in the system and is used for supporting the second user interface as well.

As a result, the spontaneous use display mode will actually increase power consumption, not reduce it. The spontaneous use mode allows only the main display backlight to be turned off. Instead, all of the components above line 80 in Figure 8 must be turned on. Hollon is not directed to reducing power but instead to enhancing convenience through the additional external display and buttons.

Similarly Umina is also not directed to reducing power. As discussed above, Umina is directed to increasing processing capability. Neither system has a low-power mode, nor a low-power subsystem to support such a mode.

In paragraph 27 of the rejection, the Examiner characterizes elements in Umina as [low-power], but has already acknowledged in paragraph 4 that Umina does not disclose low power operations. Claim 38, for example, recites, " a low-power subsystem in operation when the computer system enters the low-power mode."

Beyond the lack of any low-power functionality in either reference, Claim 38 has a low power subsystem that includes: "[1] a low power processor, [2] a low power subsystem memory and [3] an external interface," "the low power processor providing access to the computer system when the computer system is in the low power mode." The Examiner can perhaps pluck the dual processors from Umina and the external interface from Hollon, but there remain still two important distinctions.

First, there is no low-power subsystem memory in either reference. Hollon has no memory other than the main memory 82. Umina has two memories but these are shared by the two processors and the connections are swapped and reversed depending on the circumstances. Neither memory can be assigned to either processor.

Second, there is no access to the computer system when it is in low-power mode in either reference.

For these three reasons, the rejection of Claim 38 is inappropriate and should be reversed. The same can be said for Claim 51 which contains similar limitations and also to the other rejected claims that depend from either Claim 38 or 51.

Contrary to the Examiner's suggestion, there is nothing in Hollon to suggest adding the Umina low-power processor and a subsystem memory (absent from either reference) to Hollon. Cost and complexity would be increased and power is not an issue in Hollon. (Adding a low-power subsystem to Hollon would not just increase the parts

count, it would significantly increase complexity as the two systems and the connections between them would have to be developed).

Similarly, there is nothing in Umina to suggest adding a redundant memory and display from Hollon. Umina already has a power management function and if an additional display were to be added it would be coupled to the already common system bus just as it is in Hollon.

The Examiner suggests that it would be obvious to add memories in order to add storage capacity. This ignores the connections between the claimed components as well as the functional limitations. The claimed invention allows the main memory to be accessed even when the main system is in low power mode. There is nothing in either reference to suggest such a thing and the Examiner has provided no other grounds for obviousness.

D. Final Note: The Examiner's repeated issuance of redundant non-final rejections has denied Appellant access to this Board.

The non-final rejection of August 31, 2007 is the third non-final rejection in response to an Appeal Brief. All three of these rejections present only minor variations from the original final rejection March 16, 2005 from which Applicants originally appealed. None of the three rejections have cited any new references. This is tantamount to an abuse of the Office's procedural rules which are designed to accommodate the withdrawal of a rejection in favor of a new and different rejection.

The repeated refusal of the Examiner to either file an Examiner's Answer or to allow the application has significantly damaged Appellant's rights of access to this Board. It has also significantly slowed the disposition of this application. Appellant respectfully request that the Examiner be induced to either submit an Examiner's Answer or to allow all of the pending claims.

VIII. CONCLUSION

Appellants respectfully submit that all the appealed claims in this application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

Please charge any shortages and credit any overpayment to out Deposit Account No. 02-2666.

Respectfully submitted,

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Date: November 28, 2007

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IX. APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(7))

29. A method comprising:

transitioning a central processing unit (CPU) of a computer system into a low power mode, the computer system having a memory,

activating a low power subsystem when the CPU enters the low power mode, the low-power subsystem including a low power processor, an external interface and a low power memory;

independent of the CPU, using the low power processor of the low power subsystem to access data contained within the computer system memory; and

providing the accessed data through the external interface of the low-power subsystem.

30. The method of Claim 29, wherein accessing data comprises accessing data through a shared database of the low-power subsystem, the method further comprising storing at least a partial copy of data accessed from the computer system memory in the shared database.

31. The method of Claim 29, wherein accessing data contained within the computer system memory comprises accessing data contained within a disk drive unit.

32. The method of claim 31, wherein the data contained in the shared database includes multimedia data.

33. The method of claim 29, further comprising accessing data from a network via the external interface of the low-power subsystem.

34. The method of claim 33, wherein accessing data from the network comprises accessing data from the network using a wireless interface.

35. The method of claim 33, wherein accessing data from the network comprises accessing data from ~~is~~ an electronic store allowing an electronic purchase.

36. The method of claim 29, wherein providing the accessed data through the external interface comprises presenting the data accessed to a user via a display of the external interface of the low-power subsystem.

37. The method of claim 29, wherein providing the accessed data through the external interface comprises presenting the data accessed to a user via an audio medium of the external interface of the low-power subsystem.

38. An apparatus comprising:

a computer system having a central processing unit, a system memory, a mass storage device, and a user interface, the computer system having a low-power mode; and

a low-power subsystem in operation when the computer system enters the low-power mode, the low power subsystem having a low power processor, a low power subsystem memory and an external interface independent of the computer system, the low power processor providing access to the computer system when the computer system is in the low power mode and the external interface providing data accessed from the computer system externally.

39. The apparatus of Claim 38, further comprising a shared database coupled to the computer system and to the low-power subsystem and wherein the low power processes accesses the computer system through the shared database.

40. The apparatus of Claim 39, wherein the computer system memory comprises a random access memory coupled to the central processing unit, and wherein

the computer system mass storage device comprises a disk drive unit coupled to the central processing unit.

41. The apparatus of Claim 40, wherein the shared database is coupled to the disk drive unit, the shared database to store at least a partial copy of data stored on the disk drive unit.

42. The apparatus of claim 39, wherein data contained within the shared database includes multimedia data.

43. The apparatus of claim 38, wherein the low-power subsystem external interface comprises a wireless interface to connect with a local area network.

44. The apparatus of claim 39, wherein the low power subsystem external interface comprises a video display to display data from the shared database.

45. The apparatus of claim 38, wherein the external interface of the low-power subsystem further comprises a wireless user interface to receive verbal commands from a user.

46. The apparatus of claim 45, wherein the wireless user interface further comprises an audio headset to receive audio data transmitted from the wireless user interface.

47. The apparatus of claim 38, wherein the low-power subsystem external interface further comprises an interface to transmit data to a cellular phone.

48. The apparatus of claim 38, wherein the computer system comprises a main screen and the low-power subsystem comprises a miniature display screen and wherein the low-power subsystem including the miniature display screen is activated when the main screen is closed.

49. The apparatus of claim 38, wherein the computer system comprises stored multimedia data, wherein the low-power subsystem accesses the stored multimedia data and wherein the low-power subsystem presents the multimedia data to a user through the external interface.

50. The apparatus of claim 49, wherein the low-power subsystem presents the multimedia data to the user over a miniature display screen of the external interface.

51. A low-power subsystem comprising:

a miniature display screen;

a user input unit;

a low-power subsystem memory; and

a low-power processor coupled to the miniature display screen, to the user input unit, and to the memory, the low-power processor providing access for the miniature display screen and the user input unit to a connected computer system when the connected computer system is in a low-power mode.

52. The low-power subsystem of claim 51 wherein the processor provides access to the computer system through a shared database, the shared database being a part of the low-power subsystem.

53. The low-power subsystem of claim 52, wherein the shared database is coupled to the computer system to store at least a partial copy of data stored in the computer system.

54. The low-power subsystem of claim 51, further comprising a wireless interface to connect to an external network.

55. The low-power subsystem of claim 51, further comprising a wireless interface to connect the user input unit and the processor.

56. The low-power subsystem of claim 51 wherein the user input unit comprises a wireless user interface to receive verbal commands from a user.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.